CMIS
BEYOND INNOVATION

CENTRE FOR MEDICAL IMAGING STUDIES

(DEPARTMENT OF ECE, GAYATRI VIDYA PARISHAD COLLEGE OF ENGINEERING (A), VISAKHAPATNAM, ANDHRA PRADESH)

SKILL-BASED WINTER INTERNSHIP ON

VERIFICATION OF DIGITAL SYSTEM USING SYSTEM VERILOG

Join our internship program to enhance your skills and accelerate career growth effectively.

LIMITED OFFER

APPLY NOW

EARLYBIRD OFFER TILL 25-JAN-2026

REGISTRATION END BY	25-Jan-2026
INTERNSHIP START DATE	26-Jan-2026
REGISTRATION FEE	~~Rs. 4000~~ Rs. 2000
MODE OF INTERNSHIP	Online (Google Meet)
TIMING OF INTERNSHIP	7:00 PM- 9:00 PM (IST)
DURATION OF INTERNSHIP	Six Weeks (26-Jan-2026 to 06-Mar-2026)

Scan to Register:

Registration link: https://forms.gle/DpoYkrVqHpZLyqup9

About the Course & it's objectives:

The Skill-based Winter Internship Program on Verification of Digital Systems using System Verilog is designed to equip researchers, students, and professionals with the essential knowledge and technical expertise required to excel in VLSI Design and Verification. Over the six-week internship period, classes will be conducted five days a week in the evening for two hours (7 PM to 9 PM IST), offering participants a flexible and structured learning experience. This comprehensive program delves into the fundamentals of digital design, hardware description languages, and advanced verification methodologies using System Verilog, one of the most powerful and widely adopted verification languages in the semiconductor industry. The internship emphasizes both theoretical understanding and practical application, ensuring participants gain real-world skills in design modelling, testbench development, and functional verification. This internship invites students, researchers, and professionals from electronics, electrical, and computer engineering backgrounds who are keen to explore the field of VLSI design and verification. Participants will benefit from a blend of interactive lectures, guided labs, and mini projects, fostering both conceptual clarity and practical proficiency. By the end of the internship, participants will be well-prepared to apply System Verilog-based verification techniques in industry-standard workflows and contribute to cutting-edge semiconductor design and verification projects

objectives:

- Understand digital system design and simulation fundamentals.
- Learn System Verilog syntax, data types, and modelling constructs.
- To develop hands-on skills in simulation, synthesis, verification, and implementation of VLSI circuits using industry-standard EDA tools
- Familiarize participants with industry-standard verification tools and workflows.
- Prepare them for professional roles in VLSI design and verification through hands-on projects and real-time case studies.

Internship Structure:

WEEK-1	Basics of digital design using Verilog
WEEK-2	Basic requirements of System Verilog
WEEK-3	OOPS concept in System Verilog
WEEK-4	Advanced OOPS concept in System Verilog
WEEK-5	Various types of copy methods & Randomization, Constraint & IPC
WEEK-6	Mini Project & Real-Time Project Development

At the end of the program an evaluation process is conducted to issue certificates with different grades to the participants

** The Google Meet link will be sent to registered participant everyday before starting of the class**

For Inquiries Contact Us At :- cmis@gvpce.ac.in, cmisgvp@gvpce.ac.in 8519802243,9000405565